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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,775	10/30/2003	Masayuki Furuhashi	032076	7971

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EXAMINER	
SMOOT, STEPHEN W	
ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 05/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,775	FURUHASHI ET AL.	
	Examiner	Art Unit	
	Stephen W. Smoot	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 October 2003 and 21 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *1-7,20,22 and 24* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-19,21,23 and 25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10-30-03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office action is in response to application papers filed on 30 October 2003 and to applicant's election filed on 21 March 2005.

Election/Restrictions

1. Applicant's election without traverse of species E in the reply filed on 21 March 2005 is acknowledged. Currently, claims 8-19, 21, 23, 25 are readable on species E. Claims 1-7, 20, 22, 24 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to nonelected species, there being no allowable generic or linking claim.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The following title is suggested: Method for Fabricating a Semiconductor Device that Includes Using a Compound that Contains Silicon and Nitrogen to Form an Insulation Film of SiN, SiCN, or SiOCN.

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

4. Claims 9-10, 21 are objected to because of the following informalities:

In claim 9, line 7, change "a dopant" to --dopant-- to correct grammar;

In claim 10, line 9, change "anistoropically" to --anisotropically-- to correct spelling; and

In claim 21, line 4, change "siedewall" to --sidewall-- to correct spelling.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 9-10, 15, 21, 23, 25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 9, lines 2-5 indicate that the gate electrode is formed after the insulation film is formed. However, this limitation is not consistent with lines 10-12 of claim 9, which indicate that the gate electrode has already been formed and is then covered with the insulation film.

Claims 10, 15, 21, 23, 25 are rejected under 35 U.S.C. 112, second paragraph, because they depend on claim 9;

In claim 21, line 6, the term "dopant diffused regions" is not distinctly claimed from the same term as used in claim 9, line 7 and again in claim 21, line 8; and

In claim 23, line 9, the term "dopant diffused regions" is not distinctly claimed from the same term as used in claim 9, line 7 and again in claim 23, lines 4, 10.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent

granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 8, 16-17, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Xia et al. (US 6,153,261).

Referring to column 10, lines 44-67, Xia et al. teach a thermal CVD method for depositing a silicon nitride film (i.e. SiN) using a substrate temperature that is set at a temperature in the range of 500 to 650 degrees C. The process gases used to deposit the SiN film include bistertiarybutylaminosilane (BTBAS) precursor, molecular nitrogen (N_2), and ammonia (NH_3).

These are all of the limitations set forth in claims 8, 16-17, 19 of the applicant's invention.

9. Claims 8-11, 15-17, 19, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Arghavani et al. (US 2004/0033677 A1).

Referring to Figs. 3A to 3M and paragraphs [0013] to [0038], Arghavani et al. disclose a method for forming a field effect transistor that includes the following features:

- A gate dielectric (319) formed on a semiconductor substrate (300) and underneath a gate electrode (318) as shown in Fig. 3I;
- Shallow source/drain extension regions (340) implanted into the top substrate surface as shown in Fig. 3J;

- Silicon oxide layer (341) and silicon nitride layer (342) sequentially deposited over the gate structure as shown in Fig. 3K;
- The silicon nitride layer (342) can be formed by thermal CVD at a substrate temperature between 500 and 650 degrees C using bistertiarybutylaminosilane (BTBAS) precursor, molecular nitrogen (N_2), and ammonia (NH_3) process gases as described in paragraph [0026];
- The silicon nitride layer (342) and silicon oxide layer (341) are then anisotropically etched to form spacers (344) as shown in Fig. 3L; and
- Deep source/drain regions (348) are then implanted in a self-aligned manner as shown in Fig. 3M.

These are all of the limitations set forth in claims 8-11, 15-17, 19, 21 of the applicant's invention.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) as applied to claim 11 above, and further in view of Moore (US 2002/0111039 A1).

As shown above, Arghavani et al. anticipate claim 11 of the applicant's invention. However, Arghavani et al. lack the further limitations to claim 11 as set forth in claim 12, which are directed to burying an interconnect in a further another insulation film. Moore teaches the formation of a BPSG insulator layer (120) over a substrate (112) that includes gate stacks (116) with spacers (117), selectively etching a contact opening (124) through the BPSG layer (120) with respect to the spacers (117), and providing a conductive plug (130) in the contact opening (124) (see Fig. 4 and paragraph [0034])).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al. and Moore in order to form conductive plugs through an insulating layer, as taught by Moore, for making electrical connections to the source/drain regions of Arghavani et al. Moore recognizes that by selectively etching their BPSG layer with respect to the spacer material, electrical shorting between the conductive plugs and the gate electrodes will be avoided (see paragraph [0034]).

12. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Xia et al. (US 6,153,261) as applied to claim 8 above, and further in view of Huang et al. (US 6,077,769).

As shown above, Xia et al. anticipate claim 8 of the applicant's invention. However, Xia et al. lack the further limitations to claim 8 as set forth in claims 13-14, which are directed to forming an interconnect in a further another insulation film. Referring to Figs. 2A-2G and column 3, line 14 to column 4, line 49, Huang et al. teach a method of forming an interconnect over a substrate with MOS transistors (not shown) located on the substrate. IMD layers (114, 124) that can be silicon dioxide (i.e. an another insulation film and a further another insulation film) and a hard mask layer (126) that can be silicon nitride (i.e. an insulation film) are sequentially formed over the substrate (100) as shown in Fig. 2A. Interconnect holes (125, 135a) are then formed in the IMD layer (124) and the hard mask layer (126) as shown in Fig. 2E. The interconnect holes are than filled with a metal layer (130), which includes polishing back the excess metal by CMP to the hard mask layer (126) as shown in Fig. 2F. Regarding claim 14, the same method can be used to form additional interconnect levels (see column 4, lines 38-39), in which case the insulation film can correspond to a hard mask layer that overlies the interconnect (130) of Fig. 2F.

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Xia et al. and Huang et al. in order to form the hard mask layer of Huang et al. by using the silicon nitride CVD method as taught by Xia et al. Xia et al. recognize that the use of BTBAS as the silicon source for their CVD method has the advantage of an increased deposition rate (see column 2, lines 29-41).

13. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Xia et al. (US 6,153,261) as applied to claim 8 above, and further in view of Luo et al. (US 2003/0059535 A1).

As shown above, Xia et al. anticipate claim 8 of the applicant's invention. However, Xia et al. do not teach or suggest using a hydrazine compound or an azido compound as the second raw material, which is the further limitation to claim 8 set forth in claim 18 of the applicant's invention. Luo et al. teach that hydrazine can be used as an alternative nitrogen source to ammonia for depositing SiN layers (see paragraphs [0051] and [0052]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify the CVD method of Xia et al. by substituting hydrazine for ammonia as taught by Luo et al. Luo et al. recognize that hydrazine is an alternative to ammonia as a nitrogen source for depositing SiN layers (see paragraph [0052]).

14 Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) as applied to claim 9 above, and further in view of Lee et al. (US 2002/0151145 A1).

As shown above, Arghavani et al. anticipate claim 9 of the applicant's invention. However, Arghavani et al. lack the further limitations to claim 9 as set forth in claim 23, which are directed to using another sidewall spacer as a mask for implanting deeper dopant diffused regions and subsequently removing the mask by etching. Referring to

Figs. 1-6 and paragraphs [0011] to [0022], Lee et al. disclose a CMOS fabrication method that includes using sacrificial spacers (22a, 22b) as a mask for implanting deep source/drain regions (24a, 24b), removing the sacrificial spacers by etching, then implanting shallow source/drain extension regions (26a, 26b) as well as halo regions (28a, 28b), and then forming final sidewall spacers (30a, 30b).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al. and Lee et al. in order to use sacrificial spacers to form the deep implants first, as taught by Lee et al., in the transistors of Arghavani et al. Lee et al. recognize that the deep implants can be annealed prior to forming the halo regions and thereby minimizes diffusion of halo dopants from the subsequently formed halo regions (see paragraph [0028]).

15. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Arghavani et al. (US 2004/0033677 A1) as applied to claim 9 above, and further in view of Chatterjee (US 2003/0102512 A1).

As shown above, Arghavani et al. anticipate claim 9 of the applicant's invention. However, Arghavani et al. lack the further limitations to claim 9 as set forth in claim 25, which are directed to forming pocket regions. Chatterjee teaches a pMOS device (12) with n-type pocket regions (31) formed adjacent to p-type source/drain extensions as shown in Fig. 1, which implies that the pocket regions (31) are formed prior to the formation of sidewall insulators on the pMOS gate stack (34) (also see paragraph [0019]).

Therefore it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine the teachings of Arghavani et al. and Chatterjee in order to form pocket regions, as taught by Chatterjee, in the transistors of Arghavani et al. Chatterjee recognizes that pocket implants effectively reduce the sensitivity of the threshold voltage to the channel length of a field effect transistor (see paragraph [0019]).

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Laxman et al., Weimer et al., Bu et al., and Chakravarti et al. teach CVD methods for forming silicon-containing insulating layers that utilize BTBAS as the silicon source material.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen W. Smoot whose telephone number is 571-272-1698. The examiner can normally be reached on M-F (8:00 am to 4:30 pm).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr. can be reached on 571-272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sws

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